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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Whitman et al.

Serial No.: 09/542,783

Filed: April 4, 2000

For: SPIN COATING FOR MAXIMUM
FILL CHARACTERISTIC YIELDING A
PLANARIZED THIN FILM SURFACE

Confirmation No.: 6870

Examiner: B. Kebede

Group Art Unit: 2823

Attorney Docket No.: 2269-4294US
(98-1208.00/US)

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REPLY BRIEF

Mail Stop Appeal Brief - Patents
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Attn: Board of Patent Appeals and Interferences

Sir:

This Reply Brief is being submitted in response to the Examiner's Answer dated December 16, 2005, within two months of the mailing date of the Examiner's Answer, and is in compliance with 37 C.F.R. § 41.41(a). Sections I-VI and VIII-XI were not disputed by the Examiner.

VII. ARGUMENT

A. Rejections Under 35 U.S.C. § 102(e)

It has been asserted, at page 8 of the Examiner's Answer, that the disclosure of U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi") has been mischaracterized in Appellants' explanations as to why independent claim 1 recites subject matter which, under 35 U.S.C. § 102(e), is allowable over the subject matter described in Kikuchi.

It is respectfully submitted that the disclosure of Kikuchi has not been mischaracterized.

In this regard, with respect to the requirements of independent claim 1 that material be disposed on a surface of a semiconductor device structure "so as to substantially fill . . . at least one recess, . . . material covering [the] surface having a thickness less than a depth of [the] at least one recess . . . , [and] an upper surface of at least a portion of [the] material over or within [the] at least one recess being substantially planar," Kikuchi includes no express or inherent written description that any portion of the spin-coated resist described therein is substantially planar or that the thickness of portions of the resist that cover the surface of the illustrated semiconductor device structure are less than a depth of at least one resist-filled recess therein.

The lack of express written description is readily apparent from a reading of Kikuchi. The statements that have been made in the Appeal Brief to establish that Kikuchi does not expressly or inherently describe a spin-coated resist with a substantially planar surface, and that the spin-coated resist described in Kikuchi would, in fact, have a rather non-planar surface, have not been made to misrepresent the description provided by Kikuchi. Rather, each of these statements is based upon the fact that liquids, such as resist, are known to have some surface

tension. Moreover, resists are typically viscous liquids and, thus, the surface of a resist layer may not planarize on its own. These properties of resists are evident from the facts that resists must be spin-onto semiconductor wafers and they do not flow off semiconductor wafers when placed thereon.

Additionally, the drawings of Kikuchi are merely simplified representations that cannot be relied upon to establish the Examiner's assertion Kikuchi discloses a spin-coated resist with a substantially planar surface or the thickness of resist over a semiconductor device structure relative to the depth of a recess in the semiconductor device structure. This reasoning is well-founded in the patent laws, as set forth in the Appeal Brief.

Further, nothing more than the language that appears in independent claim 1 has been argued by Appellants.

It has been asserted at page 10 of the Examiner's Answer that nothing in claim 1 specifies quantitative or qualitative measurement or degree of planarization. It is respectfully asserted that the claim 1 recitation of "substantially planar" is sufficient to instruct one of ordinary skill in the art. Additionally, It was submitted on page 18 of the Examiner's Answer that *Playtex Products Inc. v. Proctor & Gamble Co.*, 73 USPQ2d 2010, 2015 (Fed. Cir. 2005) be considered with respect to the meaning of "substantial" or "substantially planar." It is noted that requiring a "degree of planarization" of "substantially planar" would be analogous to placing a numerical limit on the planarization – an approach specifically condemned by the *Playtex Products* court. See *Id.* ("The term "substantial" is a meaningful modifier implying "approximate," rather than "perfect.") But the definition of 'substantially flattened surfaces' adopted by the district court

introduces a numerical tolerance to the flatness of the gripping area surfaces of the claimed applicator. That reading contradicts the recent precedent of this court, interpreting such terms of degree.” (citation omitted)).

It is further asserted on page 10 of the Examiner’s Answer that claim 1 does not recite a planarization process that can be different from that of Kikuchi. It is respectfully submitted that such a concern is moot as Kikuchi does not describe expressly or inherently all the elements of claim 1.

With respect to the 35 U.S.C. § 102(e) rejection of claim 2, the Examiner has asserted that Figs. 2 and 3, as well as the accompanying text, of the above-referenced application are the sole sources of support in the above-referenced application for the recitation “substantially fill[ing] . . . at least one recess without substantially covering [a] surface” of a semiconductor device structure. Examiner’s Answer, pages 11-12. The Examiner then reproduces FIGs. 6E, 6F, and 16D-16F of Kikuchi to illustrate similar subject matter.

To provide a nonlimiting example of a process within the scope of claim 2, the as-filed specification of the above-referenced application, at page 6, lines 18-30 (*see, especially, lines 26-27*), quite clearly explains that “the surface of [a] semiconductor substrate [may] remain[] substantially uncovered by . . . mask material” when material is introduced into recesses that have been formed in the semiconductor substrate. It is not necessary to subsequently remove material from the surface of the semiconductor substrate, which amounts to substantially filling without substantially covering.

Figs. 2, 3, 6E, 6F, and 16D-16F of Kikuchi show processes in which material is introduced into the recesses of a semiconductor device structure *and* applied to the surface thereof. Thus, the disclosure of Kikuchi is limited to processes in which recesses in a semiconductor substrate are substantially filled while the surface of the semiconductor substrate is substantially covered. The material that covers the surface then has to be removed by a separate process. *See e.g.*, col. 18, lines 3-5; col. 40, line 66, to col. 41, line 1.

Kikuchi, therefore, lacks any express or inherent description of the subject matter recited in claim 2.

(B) Rejections Under 35 U.S.C. § 103(a)

It has been asserted that one of ordinary skill in the art would have been motivated to combine the teachings of Kikuchi with those of U.S. Patent 6,117,486 to Yoshihara (hereinafter “Yoshihara”) to render the subject matter recited in claims 3-7 unpatentable. Examiner’s Answer, page 15.

While the broad teachings of Kikuchi and Yoshihara are similar—they both relate to spin-on processes for applying resist to semiconductor device structures, neither of these references teaches or suggests that at least a portion of a surface of material that has been introduced into at least one recess of a semiconductor device structure may be substantially planar, as required by independent claim 1. *See Appeal Brief*, pages 13-15.

Yoshihara teaches that by spinning a semiconductor wafer at high speeds (“as low as 2000 rpm”; col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds,

the wafer can be coated with material in such a way that the material layer has a substantially *uniform thickness*. Yoshihara does not ever discuss the effects of Yoshihara's techniques upon a semiconductor wafer with recesses. Clearly, it is not possible for a layer which has a substantially *uniform thickness* and which is formed over a nonplanar surface to have a planar surface.

While Kikuchi does teach a recess in a semiconductor wafer, it is respectfully submitted that neither Yoshihara nor Kikuchi supplies any motivation for one of ordinary skill in the art to apply teachings from Yoshihara to Kikuchi in such a way as to introduce material into recesses of a semiconductor substrate in such a way that the material within the recesses has a substantially planar upper surface.

Additionally, Yoshihara does not teach or suggest that re-increasing of the rate of spinning of the substrate is effected gradually, as recited in claim 3. Rather, Yoshihara merely teaches and suggests that the rate of spinning is re-increased.

Further, Kikuchi and Yoshihara both lack any teaching or suggestion of the specific spinning rate recited in claim 5.

Therefore, a *prima facie* case of obviousness has not been established against the subject matter recited in any of claims 3-7.

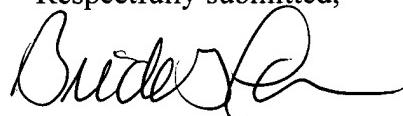
Claims 10 and 12-15, which have also been rejected under 35 U.S.C. § 103(a), are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

XII. CONCLUSION

- (A) Claims 1, 2, 8, 9, 11, 16, and 17 are allowable under 35 U.S.C. § 102(e) for reciting subject matter which is not anticipated by that the subject matter taught in Kikuchi;
- (B) Claims 3-7 are nonobvious under 35 U.S.C. § 103(a) and, thus, allowable over the asserted combination of teachings from Kikuchi and Yoshihara;
- (C) Claim 10 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over that taught in Kikuchi, in view of teachings from Lin;
- (D) Each of claims 12-15 is allowable under 35 U.S.C. § 103(a) for reciting subject matter which is allowable over that taught in Kikuchi, in view of the teachings of Park; and
- (E) Claims 18-87 should be returned to consideration and allowed.

Accordingly, reversal of the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 and of the 35 U.S.C. § 103(a) rejections of claims 3-7, 10, and 12-15 is respectfully requested, as is the allowance of each of these claims and of claims 18-87.

Respectfully submitted,



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